

REMARKS/ARGUMENTS

The present amendment is responsive to the Final Office Action dated November 19, 2009. Claims 1, 10 and 25 have been amended. No new matter has been introduced by these amendments. Claims 1-39 are again presented for the Examiner's consideration in view of the following remarks. The rejections will be addressed in view of the claims as currently presented. A petition for a two (2) month extension of time is submitted herewith.

Reexamination and reconsideration of the above-identified application, pursuant to and consistent with 37 C.F.R. § 1.116 and in light of the following amendments and remarks, are respectfully requested. Good cause exists for the entry of this amendment in accordance with 37 C.F.R. § 1.116.

Claims 1-33 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-3, 8-12, 19-22, 24-27, and 32-33 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,141,762 (*Nicol*) in view of U.S. Patent No. 6,345,362 (*Bertin*). Claims 4-7, 13-18, and 28-31 were rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Bertin*, and further in view of U.S. Patent No. 5,913,068 (*Matoba*). Claim 23 was rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Bertin* and further in view of U.S. Patent Publication No. 2002/0091954 (*Rhee*). Claims 34-35, and 38 were rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Matoba*. And claims 36-37, and 39 were rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Matoba*, and further in view of *Bertin*. Of the claims rejected, claims 1, 10, 25 and 34 are independent.

Applicant respectfully traverses these rejections as discussed in detail below.

Several additional rejections have been presented for non-statutory obviousness-type double patenting against claims 1, 10 and 25 based upon purportedly similar claim language in counterpart application 10/849,623 ("The '623 application"). A similar rejection against claim 37 was made over the '623 application in view of U.S. Patent No. 5,913,068 ("Matoba"). Applicant traverses the rejections. Applicant notes that the instant application was filed two months prior to the '623 application; therefore, the non-statutory obviousness-type double patenting rejections may be inappropriate in the instant case. See M.P.E.P. § 804(I)(B)(1). In addition, as these rejections are merely provisional, they will be addressed upon allowance of either case.

Furthermore, the Office Action asserts "[a]pplicant acknowledges that the double patenting rejections made by the Examiner are not overcome. Therefore, these rejections are not withdrawn. Applicant is advised to file a terminal disclaimer to overcome these double patenting rejections." (Final Office Action, p.27, numbered section 46.) This assertion is erroneous. Applicant has made no such acknowledgement. Rather, as indicated in the amendment of July 13, 2009, such rejections are merely provisional. As such, the merits of the rejections need not be addressed at this time. Appropriate correction of the assertion is requested in the next Office communication.

Turning to the § 112, second paragraph rejection, the Office Action asserts that "[a]s to claims 1, 10, and 25, the limitation of "commanding the sub-processing units that are not scheduled to perform any tasks because of the reallocation into a low power consumption state" is not grammatically correct and is unclear of its meaning." (Final Office Action, p.2, numbered section 3.) Applicant respectfully disagrees with this assertion and submits the claims as previously presented were grammatically correct and clear. Nonetheless, in order to advance prosecution, independent claims 1, 10 and 25 have been amended as set forth above. In view of this, applicant

respectfully requests that the § 112 rejection be withdrawn.

Turning to the rejections based upon prior art, applicant notes that certain features of claims 1, 10 and 25 are related as they pertain to monitoring processor tasks and loads of processors in a multi-processor system. Generally speaking, some of the tasks are reallocated so that at least one processor is not scheduled to perform a task, which permits such processors to enter a low power consumption state.

The rejection of claims 1, 10 and 25 admits that *Nicol* does not disclose at least one processor not being scheduled to perform a task and having such processor enter a low power consumption state. (See Office Action, p.14, numbered section 12.) According to the rejection, *Bertin* "teaches a main CPU with a plurality of functional units (sub-processors) that lowers the power consumptions state to a lower or lowest level of any of the functional units that are not scheduled to be used in execution (col. 4, lines 54-61, col. 3, lines 49-54, Abstract)." (Office Action, p.14, numbered section 12.)

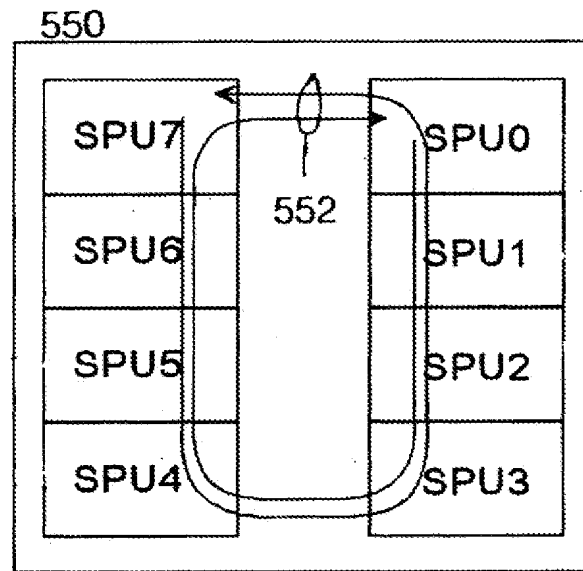
As best understood, the system of *Nicol* is configured "to equalize processing load among the chips" (2:23-24) and "to allocate that tasks to the available processors in order to balance the computation" (3:17-18). An "intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented ... among all of the PE's" (3:19-21).

In contrast, *Bertin* discloses minimizing the power level of processors which do not have an instruction to execute. As best understood, *Bertin* determines whether an instruction requires a given functional unit and ensures that those functional units are employed. (See, e.g., 2:28-43.) Here, if a functional unit is not required, its power level may be minimized. (See 4:51-65.) Applicant respectfully submits that this is not within the broadest reasonable interpretation of independent claims 1, 10 and 25, in contrast to what is asserted

in the rejection. (See numbered section 48 at p.27 of the Office Action.)

As best understood, *Nicol* and *Bertin* operate in two fundamentally different ways, and there is no proper motivation to combine their teachings as set forth in the rejection. In order to incorporate *Bertin's* teachings into *Nicol*, certain functional units/processors would be placed in a low power state. However, *Nicol* expressly discloses that its goal is to maximize parallelism among PEs and to distribute computations among the PEs. Applicant submits that powering down certain PEs is inapposite to how *Nicol* functions, and thus there is no proper motivation to combine the teachings of the references. Furthermore, *Bertin* does not disclose reallocating any tasks so that certain processors have no tasks assigned. Rather, *Bertin* appears to operate in the opposite manner, namely identifying processors that must perform certain tasks. Thus, even if one were able to combine the teachings of the cited references, the applied combination would not result in the invention of independent claims 1, 10 and 25.

Turning to independent claim 34, this claim is directed to an apparatus having a particular bus configuration. Here, the bus circularly interconnects multiple sub-processing units. This configuration is shown in FIG. 12 of the application, which is reproduced below.



The rejection of claim 34 relies on *Nicol* for a circular bus; however, as noted in the prior amendment (which is incorporated by reference for the sake of brevity), that reference does not disclose such a structure. In fact, the rejection confuses *Nicol* and *Bertin*, referring to *Bertin* as including the architecture of *Nicol* - specifically, the rejection refers to FIG. 2 of *Nicol* as being to *Bertin*.

Furthermore, the rejection appears to misread the limitation of claim 34 which requires that the sub-processing units are operable to monitor the processor tasks and reallocate at least some of the tasks based on their associated processor loads. The rejection refers to PE 100 in FIG. 2 (of *Nicol*) as being configured to perform these functions. However, the claim requires that all of the sub processing units be capable of performing the functions, not a separate PE as disclosed in *Nicol*.

Applicant submits that the applied combinations of references do not render independent claims 1, 10, 25 and 34 obvious. Therefore, applicant requests that the rejections of these independent claims be withdrawn. Furthermore, claims 2-9, 11-24, 26-33 and 35-39 depend from independent claims 1, 10, 25

and 34, respectfully, and contain all the limitations thereof. For at least this reason, applicant submits that the dependent claims are likewise in condition for allowance.

In addition to the above, with regard to dependent claim 35 the citation to *Nicol* at column 7, lines 1-3 does not address the claimed feature of arranging the sub-processing units in groups and reallocating tasks of a sub-processing unit to maintain the tasks within a given group. Rather, the cited section merely states that the PEs of a multiprocessor chip can be divided into groups and that each group can operate from its own controlled voltage supply. Thus, for at least this additional reason, applicant submits that dependent claim 35 is separately patentable over the applied combination.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have. If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

Electronic signature:

/Andrew T. Zidel/

Andrew T. Zidel

Registration No.: 45,256

LERNER, DAVID, LITTENBERG,

KRUMHOLZ & MENTLIK, LLP

600 South Avenue West

Westfield, New Jersey 07090

(908) 654-5000

Attorney for Applicant

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